



EPC C-1 G-2 / ISO 18000-6C RFID IC

Description

EM4124 is a certified EPC™ Class-1 Generation-2 (Gen2) IC and compliant with ISO/IEC 18000-6:2010 Type C.

Each chip is manufactured with a 64-bit Unique Identifier to ensure full traceability. The EM4124 has 176 bits of non-volatile memory (16 bit PC Word, 96 bit EPC Code, 32 bit Kill Password, and 32 bit Access Password), enabling the support of ISO or EPC data structures. Each chip is delivered with a 96-bit EPC encoding with pre-encoded support for Multi-vendor Chip-based Serialization (MCS).

EM4124 achieves a typical read sensitivity of -19 dBm at the chip level, which translates into a typical -21 dBm sensitivity at the tag level for a dipole-like antenna with 2 dBi gain (25us TARI, 250 kHz BLF).

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Applications

- Supply chain management
- Tracking and tracing
- Container identification
- Access control
- Asset control

IC Block Diagram

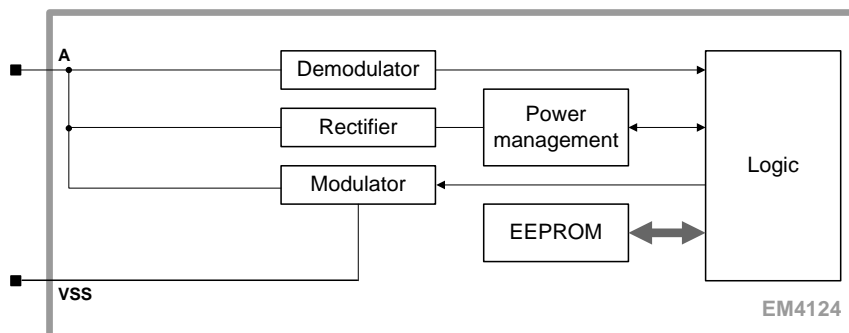


Fig. 2 IC Block Diagram

Features

- ISO 18000-6C compliant
- EPC Class-1 Gen-2 certified
- Supports Multi-vendor Chip-based Serialization
- 96-bit EPC / UII encodings are supported
- 64-bit manufacturer-programmed & locked Unique Identifier (TID / UID)
- 19 dBm (-21 dBm) typical IC (tag) read sensitivity
- 32-bit password-protected Kill command
- 32-bit password-protected Access command
- Extended temperature range (-40°C to +85°C)

Typical Operating Configuration

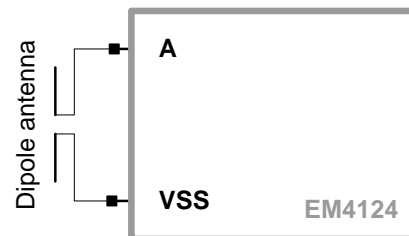


Fig. 1 Typical Operating Configuration



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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	T _{STORE}	-50	125	°C
RF power at pad A ¹⁾	P _{A_ABS}		30	dBm
Voltage on pad A	V _{A_ABS}	V _{SS} -0.2	V _{SS} +2.0	V
Voltage on pad TST1, TST3	V _{TST_ABS}	V _{SS} -0.2	V _{SS} +2.0	V
ESD hardness pad ANT, TST2 and TST3 ²⁾	V _{ESD}	-2000	2000	V

Table 1: Absolute maximum ratings
Note 1: IC impedance matched to antenna at read sensitivity

Note 2: Human Body Model

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating temperature	T _{OP}	-40	+85	°C
RF power at pad A ³⁾	P _A		20	dBm
RF carrier frequency	f _A	860	960	MHz

Table 2: Operating conditions
Note 3: IC impedance matched to antenna at read sensitivity

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range.

Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Incoming RF carrier modulation	K _M		65		100	%
Input impedance (between A and VSS) above activation threshold	Z _A	P _{DUT} = -17dBm T = 25°C f _A = 866MHz f _A = 915MHz f _A = 953MHz		25 – j276 22 – j261 20 – j251		Ω Ω Ω
Resistive load (between A and VSS) when modulator is on	R _{A_ON}	1mA into pad A T = 25°C		50		Ω
Read sensitivity for power matching (complex-conjugate matching)	P _{RD}	T = 25°C f _A =866MHz f _A =915MHz f _A = 953MHz		-19 ⁴⁾ -19 ⁴⁾ -19 ⁴⁾		dBm dBm dBm
Write sensitivity for power matching (complex-conjugate matching)	P _{WR}	T = 25°C f _A =866MHz f _A =915MHz f _A = 953MHz		-8 -8 -8		dBm dBm dBm

Table 3: Electrical characteristics
Note 4: 25 us TARI, 250 kHz BLF

Timing Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Erase / write endurance	T _{CYC}		10k			Cycles
Retention	T _{RET}	T _{OP} = 55°C	10			Years

Table 4: Timing characteristics



Functional Description

The EM4124 is used in passive UHF transponder applications operating at 860 MHz - 960 MHz. It is powered by the RF energy transmitted by the reader, which is received and rectified to generate a supply voltage for the IC. This device is in full compliance with ISO/IEC 18000-6C and is EPC™ Class-1 Generation-2 certified according to the following documents:

"ISO/IEC 18000-6:2010 Information technology – Radio frequency identification for item management – Part 6: Parameters for air interface communications at 860 MHz to 960 MHz"

"EPC Radio-Frequency Identity Protocols, Class-1 Generation-2 UHF RFID, Protocol for Communications at 860 Mhz - 960 MHz, Version 1.1.0" from EPCglobal Inc.

"EPCglobal Tag Data Standards, Version 1.6" from EPCglobal Inc.

Memory Organization

EM4124 memory is allocated to three memory banks: Reserved, TID, and EPC. The 64-bit TID / UID is programmed and write permalocked at wafer test and before customer delivery. This guarantees the uniqueness of each device on the market. The custom command GetUID allows fast access of the UID and provides more confidence in the uniqueness.

Memory name	Memory bank	Word Address	Contents	Memory type
RESERVED	00 ₂	0	Kill password	NVM
		1		
		2	Access password	
		3		
TID	10 ₂	0	TID	ROM or mapped
		1		
		2	SN	
		3		
EPC	01 ₂	0	CRC-16	RAM
		1	PC	NVM
		2	EPC	
		3		
		4		
		5		
		6		
		7		

Table 5: Memory map.

Word	0																1															
Bits (MSB first)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	ISO/IEC 15963 Allocation Class								Tag mask-designer identifier								Tag model number															
	11100010 ₂ (ROM)								000000001011 ₂ (ROM)								See definition of Tag Model Number															
Word	2																3															
Bits (MSB first)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	32-bit serial number (SN)																															

Table 6: TID / UID memory map for class identifier E2h; standard version

Tag Model Number												
Bits (MSB first)	11	10	9	8	7	6	5	4	3	2	1	0
Content	000010 ₂						Customer Number (default = 000 ₂)				000 ₂	

Table 7: Definition of Tag Model Number

Delivery State

The delivery state has the following default product configuration:

- Access Password and Kill Password are readable/writeable with a value 0000'0000'0000'0000h
- Unique Identification number (UID / TID) is programmed and write-permalocked
- EPC memory is unlocked with a default 96-bit EPC Code value 0000'0000'0000'0020'nnnn'nnnnh where nnnn'nnnn is the 32-bit serial number found in the TID memory

Commands

Three sets of commands are defined:

- Mandatory
- Optional
- Custom

Command codes

The table below shows all implemented commands in EM4124. For the description of all mandatory and optional commands, please refer to the EPCglobal Class-1 Gen-2 standard. More detailed information on custom commands is given below.

Command code	Type	Function
'00'	Mandatory	QueryRep
'01'	Mandatory	ACK
'1000'	Mandatory	Query
'1001'	Mandatory	QueryAdjust
'1010'	Mandatory	Select
'11000000'	Mandatory	NAK
'11000001'	Mandatory	Req_RN
'11000010'	Mandatory	Read
'11000011'	Mandatory	Write
'11000100'	Mandatory	Kill
'11000101'	Mandatory	Lock
'11000110'	Optional	Access
'11100000 00000000'	Custom	GetUID

Table 8: Command codes

Custom Commands and Features

GetUID

GetUID	Command code	RN
# of bits	16	16
Description	11100000 00000000	Prior RN16 or handle

Table 9: GetUID Command

The custom command GetUID is implemented as in Table 9. It allows an interrogator to read the tag's 64-bit TID / UID with a single command. A tag in Reply, Acknowledged, Open or Secured state backscatters {0', TID / UID, RN16, CRC-16} upon a GetUID command with a valid RN16 or handle (see Table 10). The state transition and link timing is the same as for the ACK command. The tag reply is analogous to the tag reply upon a Read command. A link timing example is shown in Figure 3.

	Header	UID	RN	CRC-16
# of bits	1	64	16	16
Description	0	TID / UID	RN16 (prior RN16 or handle)	CRC-16('0'+TID+RN16)

Table 10: GetUID backscatter format

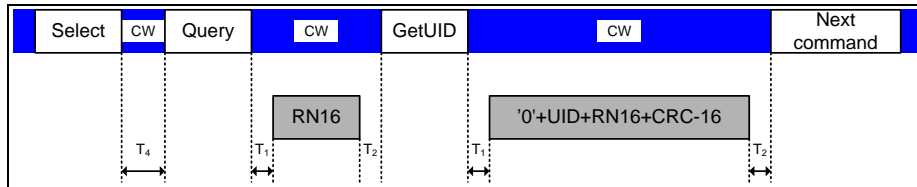


Fig. 3: GetUID backscatter timing diagram

Floor Plan and Pin Description

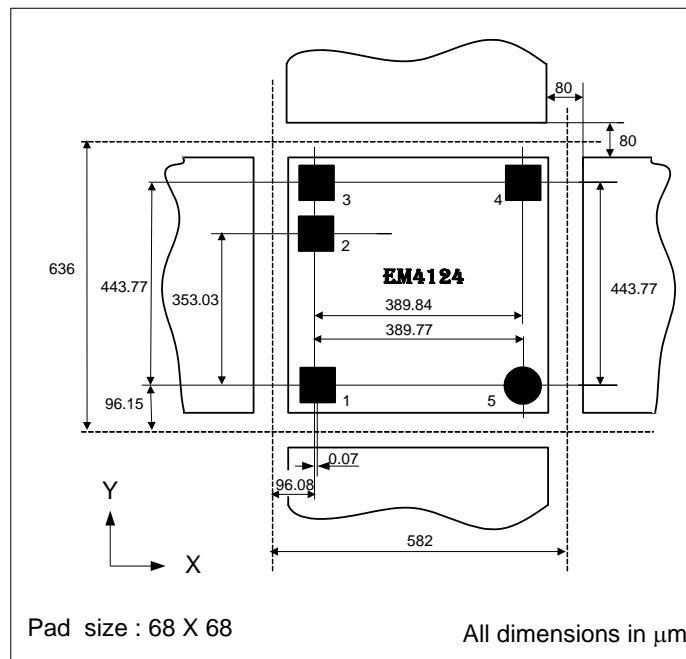


Fig. 4: Chip dimensions and pins location

Pin	Name	Pad Type	Description
1	VSS	Bumped	Antenna -
2	TST1	Un-bumped	N/A - Test purpose only
3	TST2	Bumped	N/A - Test purpose only
4	TST3	Bumped	N/A - Test purpose only
5	ANT	Bumped	Antenna +

Table 11: Pin description. Pins TST2, TST3, VSS can be shorted to ease inlay assembly.

Ordering Information

The following charts show the general offering. For detailed Part Number to order, please see the table “Standard Versions” below.

Die form

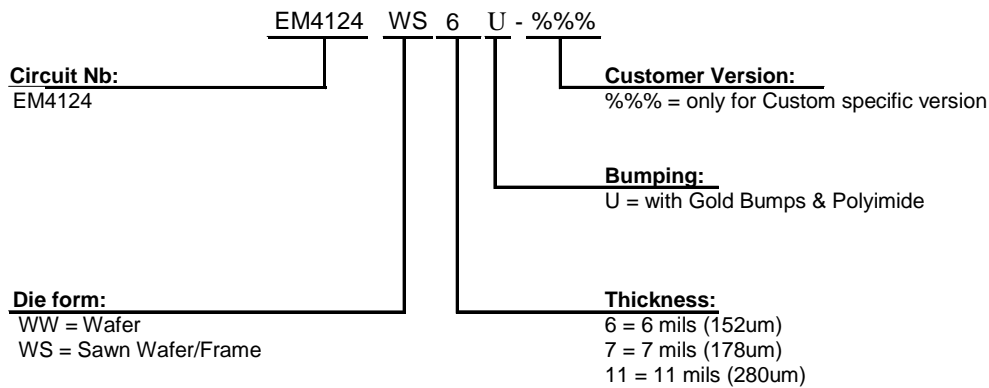


Fig. 5: Ordering information

Remarks:

- For ordering, please, use table of “Standard Version” table below.
- For specifications of Delivery Form, including gold bumps, tape and bulk, as well as possible other delivery form or packages, please, contact EM Microelectronic-Marin S.A.

Standard Versions & Samples:

The versions below are considered standards and should be readily available. For other versions or other delivery form, please contact EM Microelectronic-Marin S.A. For samples, please, order exclusively from the standard version.

Part Number	Protocol	Package/Die Form	Delivery Form
EM4124WS6U	EPC Gen2 / ISO 18000-6C	Sawn wafer / bumped die – thickness of 6 mils	Wafer sawn on frame
EM4124VXYYY-%%%	Custom	custom	Custom

Table 12: Standard EM4124 versions readily available

Product Support

Check our website at www.emmicroelectronic.com under Products/RF Identification section. Questions can be submitted to info@emmicroelectronic.com.

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