Read-only UHF RFID IC

Description

The chip is used in passive UHF read-only transponder applications. It is powered up by an RF beam transmitted by the reader, which is received and rectified to generate a supply voltage for the chip. A pre-programmed code is transmitted to the reader by varying the amount of energy that is reflected back to the reader. It implements a robust and fast anti-collision protocol. The chip is frequency independent and can be used for RF coupled applications where reading ranges in excess of 10 m and reading rates of 120 tags per second at 256 kbit/s can be attained.
The chip is backscattering data using load modulation.
Therefore the reader should be able to detect ASK and PSK modulated carrier.

Typical Applications

The chip is ideal for applications where long range, high-speed item identification is required:

- Supply chain management
- Tracking and tracing
- Access control
- Asset control
- Licensing
- Auto-tolling
- Animal tagging
- Sports event timing

Features

- Factory programmed 64 bit ID number
- High data rate: Up to 256 kbit/s
- Frequency independent: Typically used at 869 MHz, 902 - 960 MHz (versions 001 to 099)
- On-chip oscillator
- On-chip rectifier
- Low voltage operation - down to 1.0 V at ambient temperature
- Tag Talk Only protocol (TTO)
- Low power consumption
- Low cost
- -40° to +85° C operating temperature range

Benefits

- Anti-collision suited to flux monitoring
- Very low consumption
- High backscatter amplitude
- Designed for ease of antenna attachment

Typical Operating Configuration

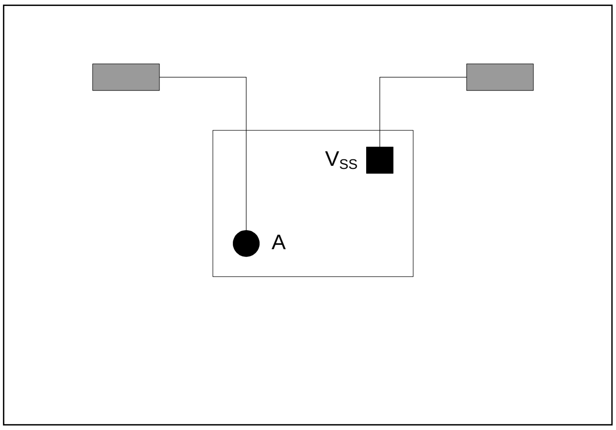


Fig. 1

UHF transponders can be implemented using an EM4123 chip and an open dipole antenna.

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum RMS current supplied into A	I_A	10 mA
Storage temperature	T_{STORE}	-55 to +125°C
Electrostatic discharge maximum to MIL-STD-883C method 3015 **Version 001 to 099**	V_{ESD}	2 KV

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all the terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating temperature	T_A	-40		+85	°C
RMS current supplied into A				10	mA

Electrical Characteristics

V_A - V_{SS} = 2.0 V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Test conditions	Min	Typ	Max	Units
Oscillator frequency	F_{OSC}	-40°C to +85°C	400	512	600	kHz
Wake-up voltage	V_{WU}	$V_A – V_{SS}$ rising	1.0	1.4	1.8	V
Static current consumption	I_{STAT}	$V_A – V_{SS}$ = 1 V		1	5	µA
Input series impedance	Zin	P_{DUT} = -12 dBm; Die form f_a = 868 MHz; f_a = 915 MHz;	 20-j530 20-j500	 40-j590 40-j560	 50-j650 50-j620	 Ω Ω
		P_{DUT} = -12 dBm; SC70 3L f_a = 868 MHz; f_a = 915 MHz; f_a = 953 MHz;		 9.6-j214 10.1-j204 9.4-j195		 Ω Ω Ω

Block Diagram

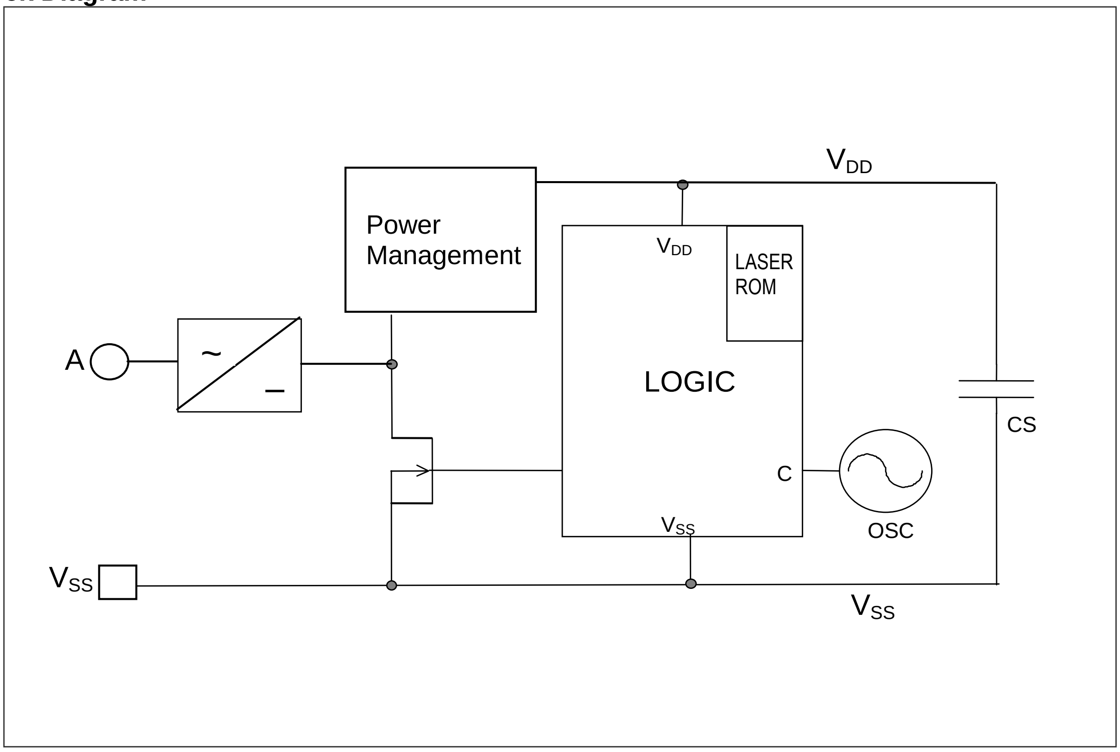


Fig. 2

Functional Description

Shunt regulator
The shunt regulator has two functions. It limits the voltage across the logic and protects the Schottky rectifier diodes.

Oscillator
The on-chip RC oscillator has a center frequency of 512 kHz. It supplies a clock to the logic and defines the data rate.

Wake-up voltage
The reset signal keeps the logic in reset when the supply voltage is lower than the threshold voltage. This prevents incorrect operation and spurious transmissions when the supply voltage is too low for the oscillator and logic to work properly. It also ensures that transistor Q2 is off and transistor Q1 is on during power-up to ensure that the chip starts up.

Modulation transistor
The N channel transistor Q2 is used to modulate the transponder antenna. When it is turned on it loads the antenna, thereby changing the load seen by the reader antenna, and effectively changing the RCS of the tag and the amount of energy that is reflected to the reader.
Q2 is active for Data Out = "1".

Antenna adaptation
The antenna attached to the pads A and V_{SS} should have an impedance at the operating frequency equal to the conjugate math of the chip's impedance. This adaptation is required for best energy transfer and maximum of reflection coefficient.

Charge preservation transistor
The P channel transistor Q1 is turned off whenever the modulation transistor Q2 is turned on to prevent Q2 from discharging the power storage capacitor (CS). This is done in a break-before-make manner, i.e. Q1 is first turned off before Q2 is turned on, and Q2 is turned off before Q1 is turned on.

LOGIC block
After the power-on reset has disappeared, the chip boots by reading a seed value into the random number generator. The least significant 16 bits of the ID (the CRC) is used as a seed.
The chip then enters its normal operating mode, which consists of clocking a 16 bit timer counter with the bit rate clock until it compares with the number in the random number generator. At this point a code is transmitted. The random number generator is clocked to generate a new pseudo random number, and the 16 bit counter is reset to start a new delay.
The width of the comparison between the 16 bit random number and the 16 bit delay count determines the maximum possible delay between transmissions (reading rate). Any one of four maximum delay settings can be pre-programmed.

Data encoding method
The transmitted code consists of an 11 bit preamble followed by the 64 code bits. The preamble consists of 8 start bits (ZEROES), followed by a SYNCH. The SYNCH consists of a LOW for two bit periods followed by a ONE.
A ONE is represented by a HIGH in the first quarter of the bit period, while a ZERO is represented by a HIGH in the third quarter of the bit period.

Timing characteristics
- Data clock: 2 x data rate
- Data out modulation duration (T_{Mod}) = $\frac{1}{4 \text{ x Data rate}}$

Down link data encoding

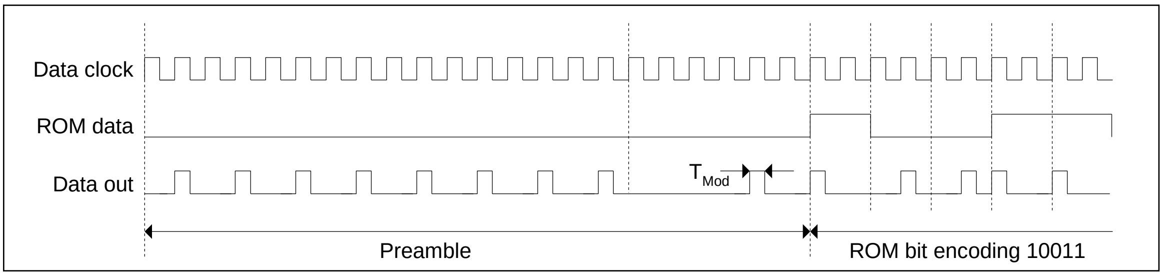


Fig. 3

ROM programming
The EM4123 contains two laser fuse ROM blocks that are pre-programmed by the foundry. The ROM blocks are split in two parts: the Code ID ROM and the Control ROM.

CODE ID ROM
This ROM contains the 64 bit ID code which is programmed by the foundry. A 32 bit UID along with a 10 bit customer code are provided to ensure a unique chip identifier (Refer to figure 4). A 16 bit CRC is provided to ensure the data integrity of the ID code (Refer to figures 4 and 5). Bit 63 is the most significant bit of the ID code and bit 0 is the least significant bit. The ID code is transmitted most significant bit first.

CONTROL ROM
The operational modes of the EM4123 are pre-programmed into the CONTROL ROM. Five standard versions are available as described in table 1.

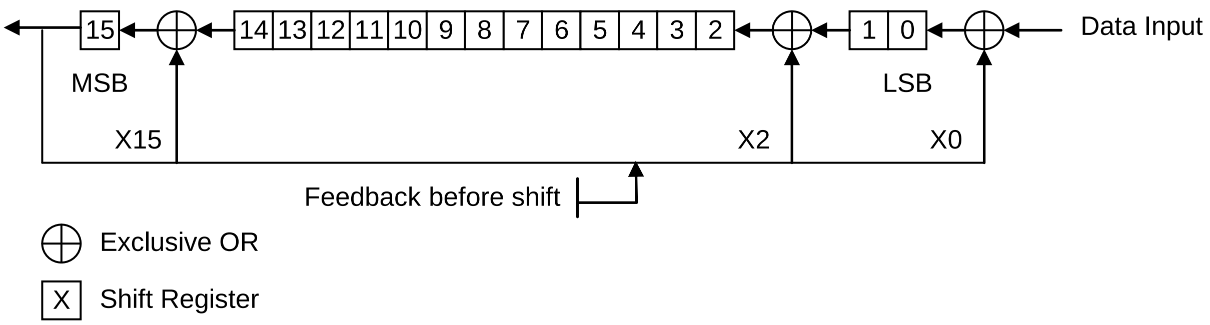
ID Code Structure

EXT	MAN	CUST	UID	CRC
Bit 63-62	Bit 61-58	Bit 57-48	Bit 47-16	Bit 15-0

EXT:	Programmed '00' to indicate 64 bit Read-Only capability
MAN:	4 bit IC manufacturer's code (0001 for EM)
CUST:	10 bit customer code. Standard 011 000 0000
UID:	32 bit unique ID
CRC:	16 bit CRC

Fig. 4

CRC Block Diagram



CRC-16 Generating polynomial = X16 + X15 + X2 + 1. The CRC is seeded with FFFF. Transmit MSB first.

Fig. 5

Application Overview

The EM4123 chip implements a fast and reliable anti-collision protocol. The chip is typically used in passive transponder applications, i.e. it does not require a battery power source. Instead, it is powered up by an RF beam transmitted by the reader, which is received and rectified to generate a supply voltage for the chip. A pre-programmed code is transmitted to the reader by varying the amount of energy that is reflected back to the reader. This is done by modulating an antenna, thereby effectively varying the radar cross section (RCS) seen by the reader.

A UHF tag can be implemented using an EM4123 chip and an antenna (typically printed). High reading distances (> 10 m) and high data rates (up to 256 kbit/s) can be achieved.

The basis of the anti-collision protocol is that tags transmit their own codes at random times to a reader. By just listening and recording unique codes when they are received, the reader can eventually detect every tag. The reader typically detects collisions by checking a CRC. Its main advantage is that the reader design is simple, and the spectrum requirement is low – a very narrow band is required.

Figure 6 shows a sequence of three transponders. The reader starts to read transponder 3 but during its data transmission, transponder 1 starts to transmit. In this case, due to the CRC check, the collision is detected and the transmission discarded. Next both transponders 2 and 3 are detected successfully and eventually transponder 1 as well. A transponder is registered only if it transmits a complete ID without any errors.

Max timing delay for ID transmit

All communication packets consist of 64 bit ID bits plus 11 header bits = 75 bits.

Calculation for the EM4123V2, i.e. data rate is 64 kbps, maximum random delay is 16 kbits.

Max random delay is 16 kbits / 64 kbps = 256 ms.
The random delay is 8 times faster on the first transmissions.
So the Max initial random delay is 32 ms.
The first transmission will occur between 16 bit clocks and the max random delay:

power-up +256µs and **power-up +32 ms**.

The *mean value* is **16 ms** for the first transmission.

Max. time to read full ID:
Max. initial Rnd delay + 75 bits @ 64 kbps

Min. delay (µs)		Max. Rnd delay (ms)		Message (ms)
		Initial	after 6 transmissions	
256	V1	8	64	1.2
256	V2	32	256	1.2
64	V3	2	16	0.3
64	V4	8	64	0.3
64	V5	32	256	0.3

Example Transmission Sequence

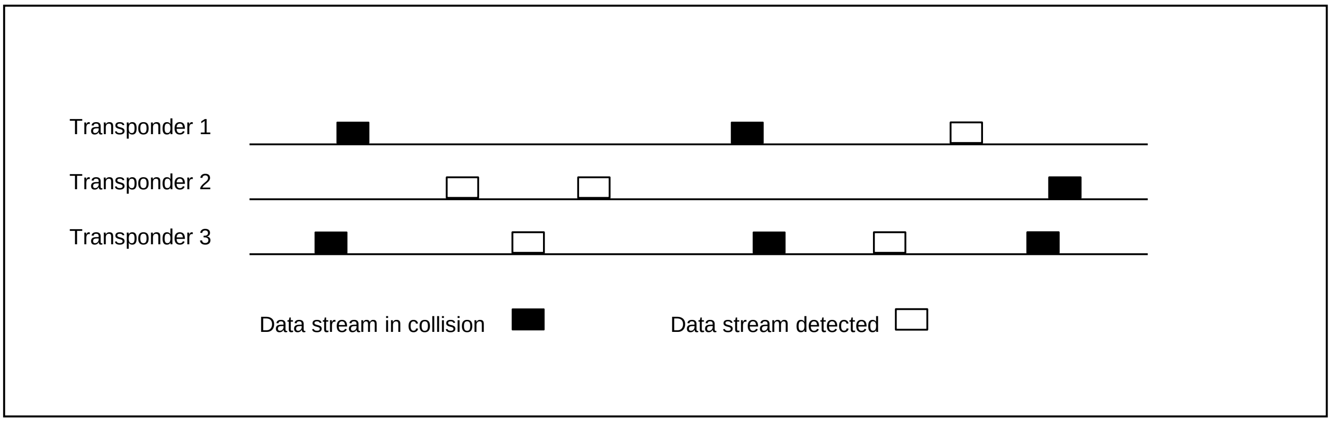


Fig. 6

Protocol Saturation

As the number of tags in a reader beam is increased, the number of collisions between transmissions increases and it takes longer to read all the tags. This process is not linear. To read twice as many tags could take more than twice as long. This effect is called protocol *saturation*. The EM4123 implements a patented technique for reducing the effects of saturation.

It is also possible to optimize the protocol for various applications (few fast moving tags vs. large numbers of slow moving tags) by setting the maximum random delay between transmissions. Four different settings are available from 1 kbits to 64 kbits. A higher setting means it will take longer to read a small number of tags, but it will take a larger number of tags to saturate the channel.

Figure 7 shows average reading times for the standard versions. Maximum reading time (3σ) for a given number of tags can be up to double the average reading time. With both V4 and V5 a minimum of 60 tags can be read in one second.

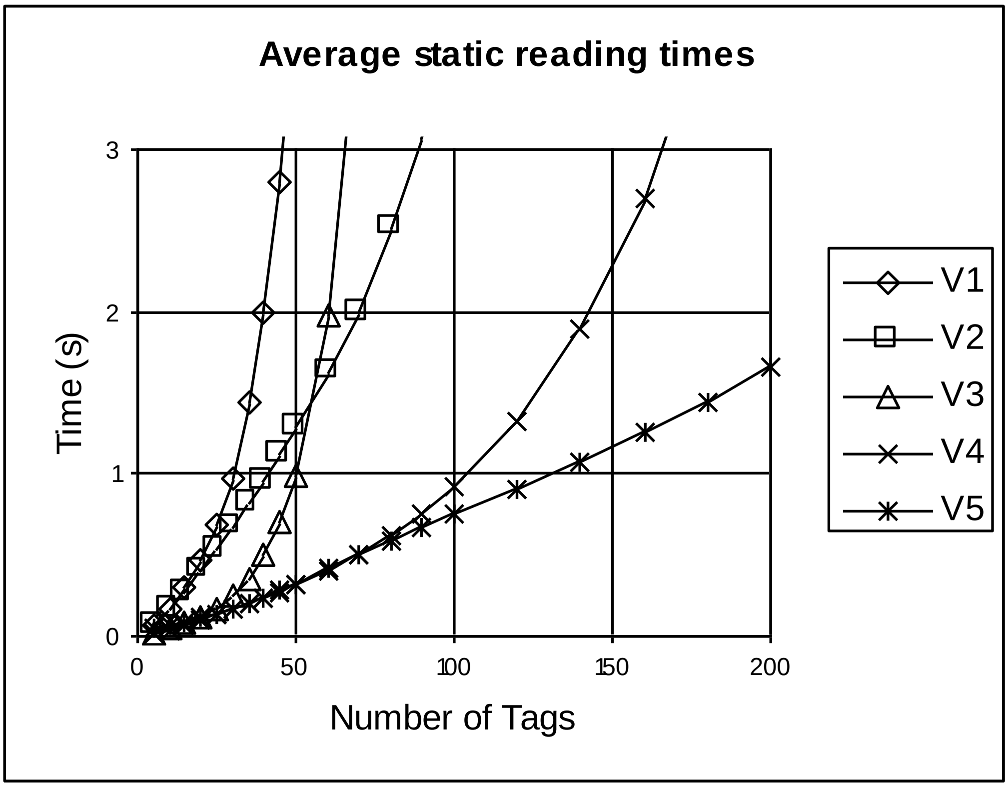


Fig. 7

Figure 8 shows average reading rate for the standard versions. V4 and V5 achieve maximum reading rates of nearly 200 tags per second.

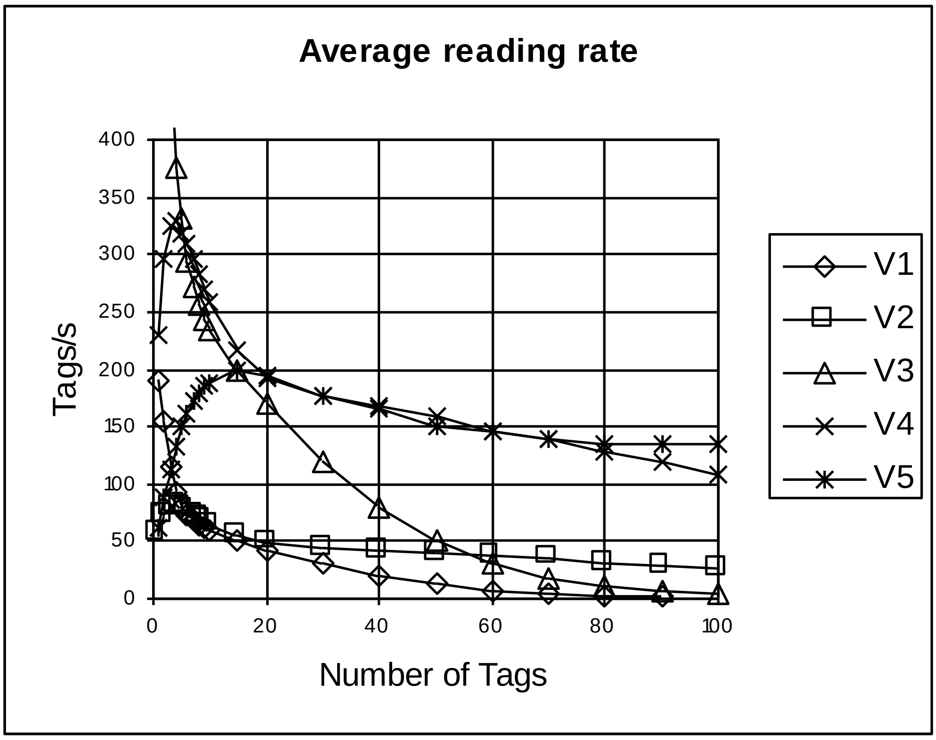


Fig. 8

Figure 9 shows maximum speeds that can be achieved with a reader that conforms to European power levels (approximately 2 meter reading range and beam width). These speeds can be more than doubled for applications in the USA.

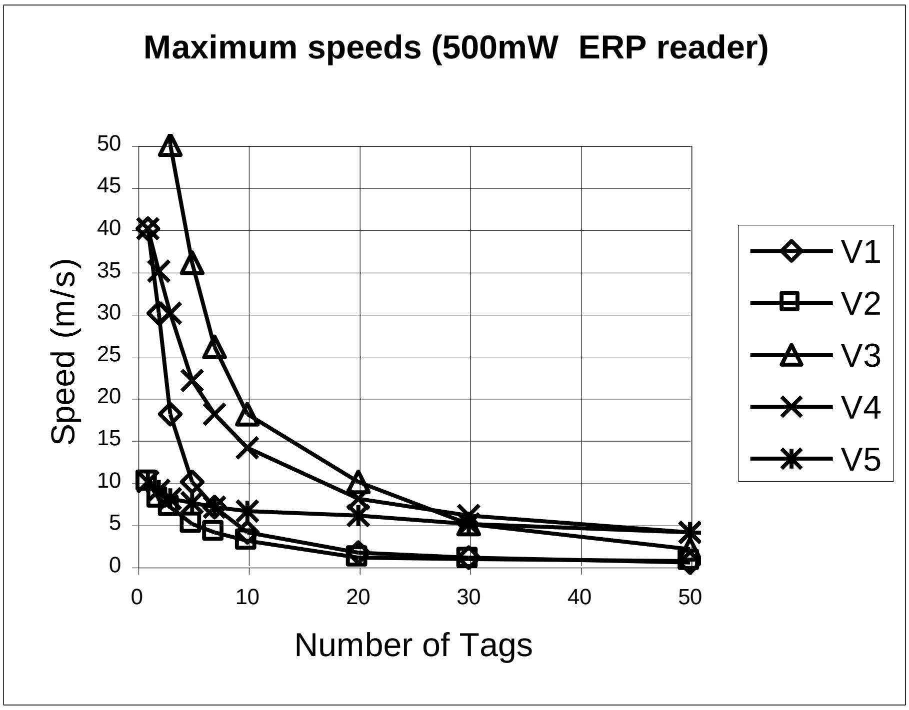


Fig. 9

V4 tags are suitable for most SCM applications. V5 tags should be used where more than 100 tags will be read simultaneously. V3 tags should be used for high-speed applications.

Version selection

The version number is a 3 digit description.
The first digit is the frequency selection;
The 2 following digits are the operational mode selection.

Vxyz

x : frequency selection
yz : operational mode

Operational mode definition

The operational modes are pre-programmed into the 5 bit CONTROL ROM. This operational mode is defined as the version number of the chip, as described in the table hereunder.

Version	Tx Data rate	Max interval
Vx01	64kbps	4k
Vx02	64kbps	16k
Vx03	256kbps	4k
Vx04	256kbps	16k
Vx05	256kbps	64k

Operating frequency selection

The operating frequency selection is done when ordering the chip.
In the version number, the first digit stands for the operating frequency for which the chip is optimized:

Version	Operating frequency
V0yz	800 MHz – 1 GHz

V0yz is often called the UHF range, or 900 MHz range

Die form information

Pad location diagram

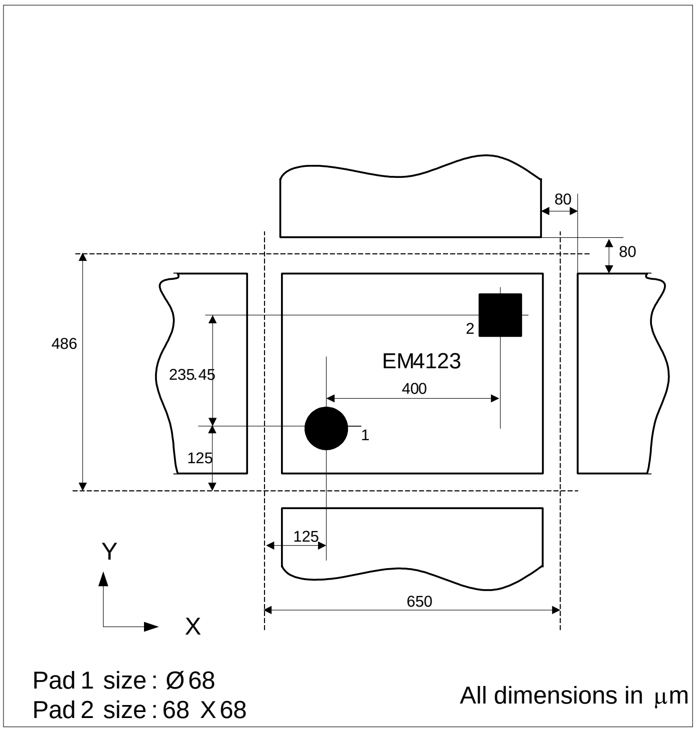


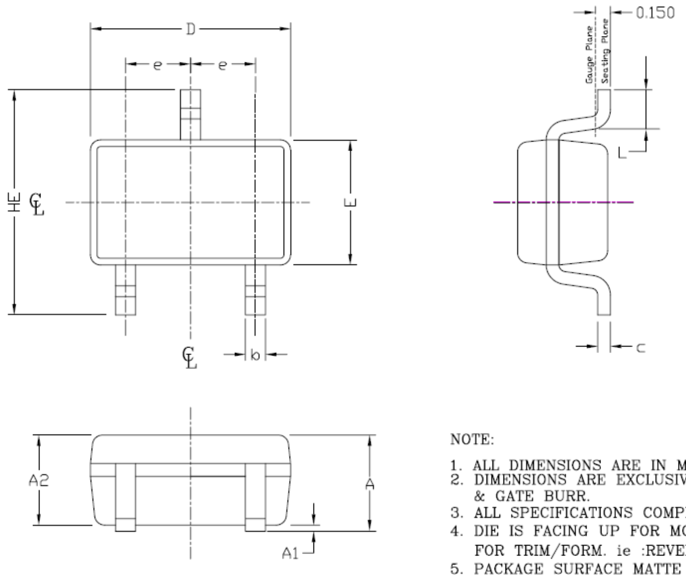
Fig. 10

Pad description

Pad	Name	Description
1	Ant +	Antenna + terminal
2	Vss	Antenna - terminal

Packaging information:

EM4123 is available in SC70 3L package on request. Please contact EM sales support for more information. EMdirect@emmicroelectronic.com



SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	2.00	2.30
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.65 BSC	
b	0.15	0.30
c	0.08	0.25
L	0.21	0.41

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & GATE BURR.
3. ALL SPECIFICATIONS COMPLY TO JEDEC SPEC MO-203 ISSUE A.
4. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM. ie :REVERSE TRIM/FORM.
5. PACKAGE SURFACE MATTE FINISH VDI 11~13.
6. THE FOOT LENGTH MEASURING BASED ON GAUGE PLANE METHOD.

Fig.11

Packaging pin-out – SC70 3L

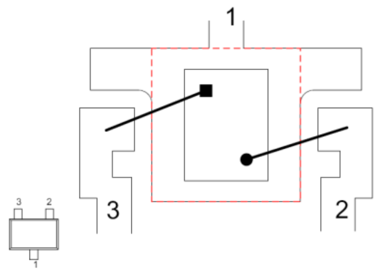


Fig.12

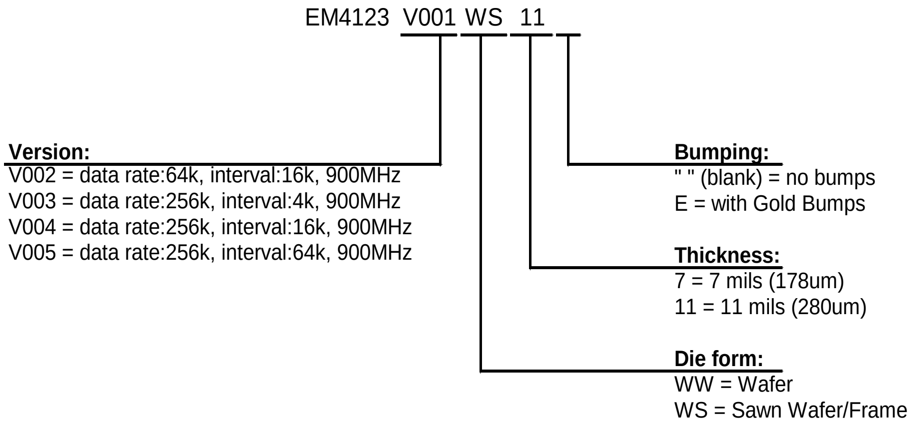
Note:

- Pad # 2 connected to Antenna terminal
- Pad #3 connected to VSS terminal

Ordering Information

The following charts show the general offering. For detailed Part Number to order, please see the table “Standard Versions” below.

DIE FORM:



Remarks:

- ❑ For ordering, please, use table of “Standard Version” table below.
- ❑ For specifications of Delivery Form, including gold bumps, tape and bulk, as well as possible other delivery form or packages, please, contact EM Microelectronic-Marin S.A.

Standard Versions:

The versions below are considered standards and should be readily available. For the other delivery form, please contact EM Microelectronic-Marin S.A.

Part Number	Version Number	Die Form	Delivery form/Bumping
EM4123V002WW11	V002	Unsawn wafer	No bumps
EM4123V002WS7E	V002	Sawn wafer	Gold bumps
EM4123V004WW11	V004	Unsawn wafer	No bumps
EM4123V004WS7E	V004	Sawn wafer	Gold bumps
EM4123V005WS11E	V005	Sawn wafer	Gold bumps

Product Support

Check our web site under Product/RF Identification & Security section. Questions can be sent to info@emmicroelectronic.com.