READ/WRITE ANALOG FRONT END IC WITH SERIAL µC INTERFACE FOR USAGE IN 125 / 134.2 KHZ RFID BASESTATION APPLICATIONS

Description

The EM4097 (previously named P4097) chip is a CMOS integrated transceiver circuit intended for use in an RFID basestation to perform the following functions:

- Antenna driving with carrier frequency to transfer energy to the transponder
- Data transfer to writable transponder by amplitude modulation (ASK) of the field (100% modulation ratio, called OOK, "on"-"off" keying)
- Data transfer from transponder by amplitude- or phase demodulation (ASK or PSK)
- µC Interface to communicate with a microprocessor

Features

- Integrated PLL system to achieve self adaptive carrier frequency to antenna resonant frequency
- Chip can be forced to run with external clock, division ratio 32
- 100kHz to 150kHz carrier frequency range
- Direct antenna driving using bridge driver
- Data transmission by OOK (100% Amplitude Modulation) using bridge driver
- Multiple transponder protocol compatibility, (Ex.: EM4102, EM4200, EM4450 and EM4205/EM4305)
- Two sampling points for demodulation, allowing extended system tolerances
- Serial µC interface for diagnosis and status control
- Very low sleep mode current consumption of 1µA typically
- USB compatible power supply range
- -40 to +85°C automotive temperature range
- Small outline plastic package SO16

Applications

- Animal ID reader
- Hand held Low Frequency reader

Read/Write Mode using internal PLL signal

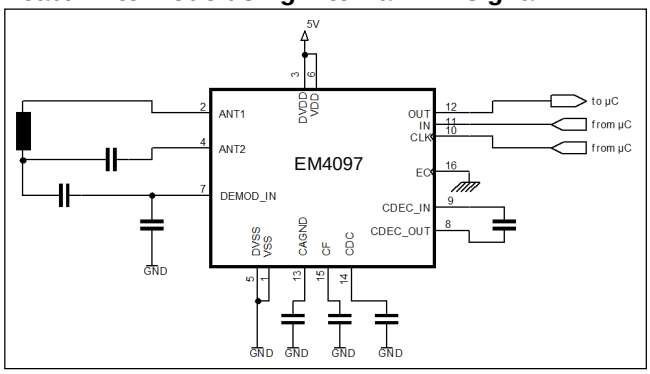

Fig. 1

Read/Write Mode using external reference signal

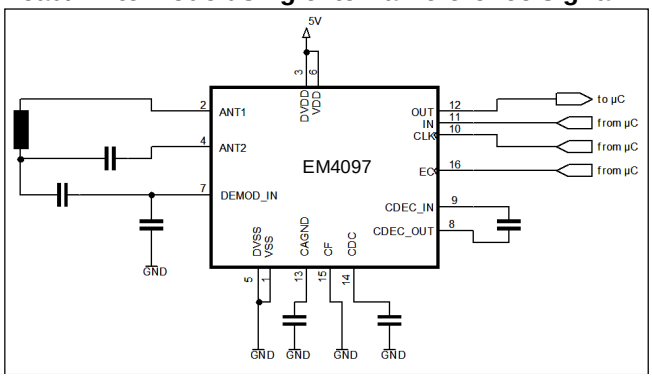

Fig. 2

Pin Assignment

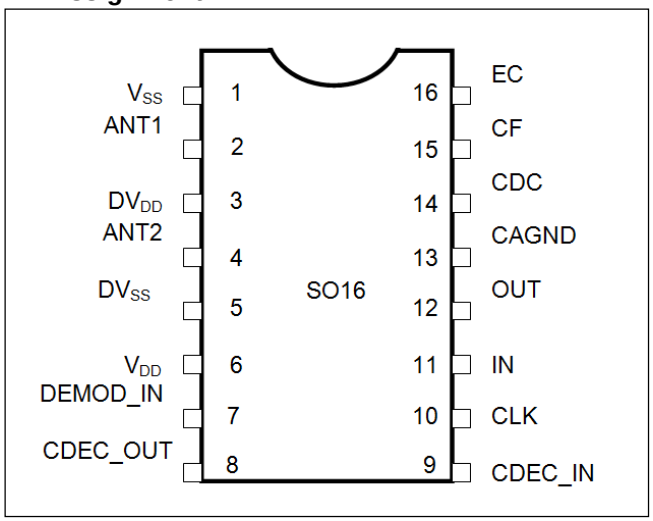

Fig. 3 Pinning Diagram

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System Principle

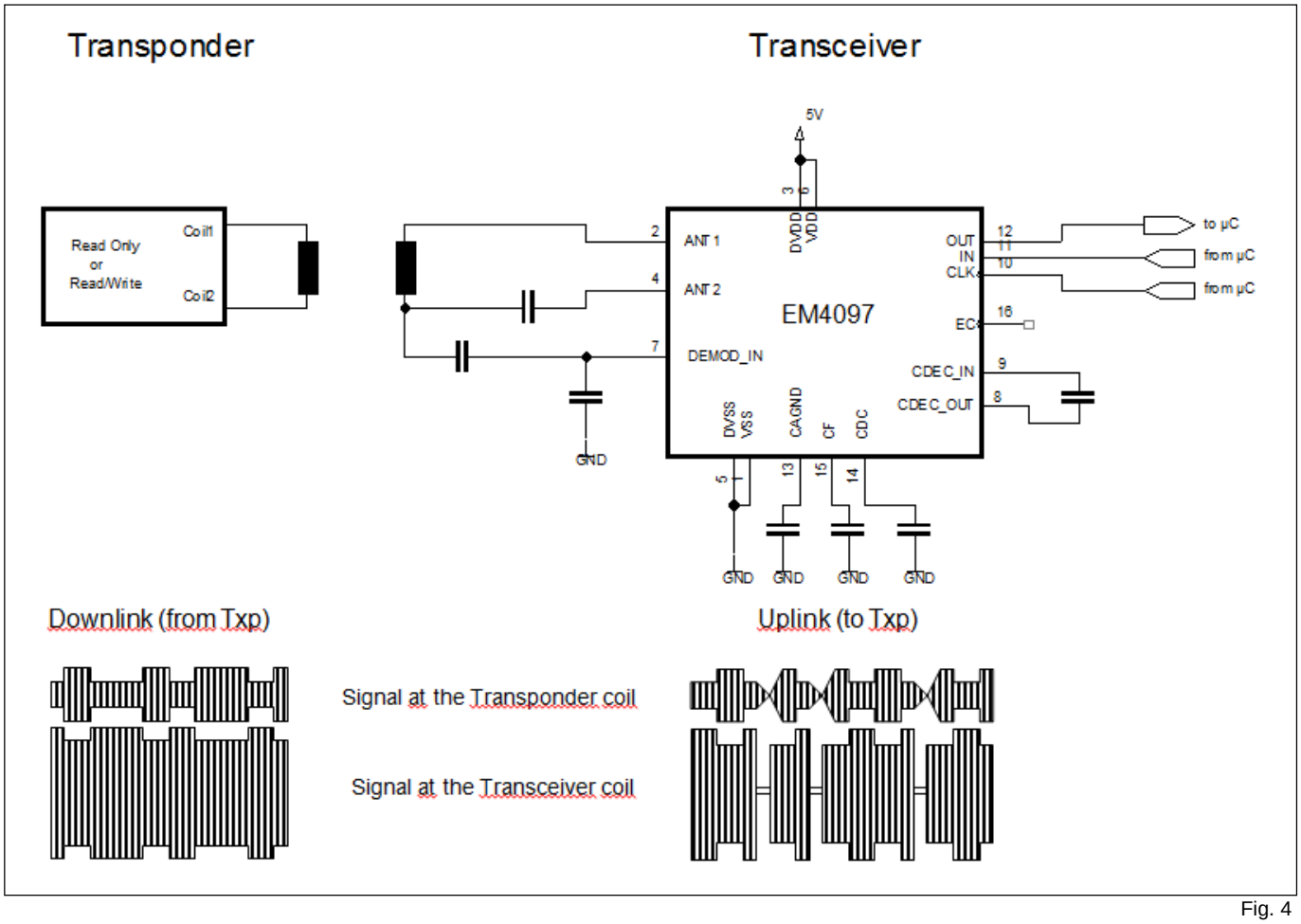

Fig. 4

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Storage temperature	T_{Store}	-55°C to +125°C
Maximum voltage at V_{DD}	V_{DDma}	V_{SS} + 6V
Minimum voltage at V_{DD}	V_{DDmin}	V_{SS} - 0.3V
Maximum voltage at other pins	V_{max}	V_{DD} + 0.3V
Minimum voltage at other pins	V_{min}	V_{SS} - 0.3V
Maximum junction temperature	T_{Jmax}	+125°C
Electrostatic discharge according to MIL-STD-883C method 3015 (pins ANT1 and ANT2)	V_{ESD_Ant}	10000V
Electrostatic discharge according to MIL-STD-883C method 3015 (other pins)	V_{ESD}	4000V
Maximum Input/Output current for each pin except V_{DD}, V_{SS}, DV_{DD}, DV_{SS}, ANT1, ANT2	$I_{Imax/Omax}$	10mA
Maximum AC peak current for ANT1 and ANT2 pins @ 100 kHz, 50% duty cycle	I_{ANTma}	400mA_p

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating junction temperature	T_J	-40		+110	°C
Supply voltage	V_{DD}	4.1	5	5.5	V
Antenna circuit resonance frequency	F_{Res}	100	125	150	kHz
Q of antenna circuit			10		
Current through ANT1 and ANT2 pins	I_{Ant}			250	mA_p
C_F (not needed if external clock is used)	** ***	*	10 100	*	nF
C_{DEC}		*	100	*	nF
C_{DC}		*	10	*	nF
C_{AGND}		100		220	nF
Thermal resistance of SO16, soldered on 1.5mm FR4 board with 35µm copper, standard footprint	R_{thJA} ****	69	70	71	°C/W

*: ±10% tolerance capacitors should be used
**: Phase demodulation with PLL is used (see Bit#1 of serial interface register)
***: Phase demodulation with PLL is not used (Bit#1 should be set to “0”)
****: Due to the antenna driver losses the internal junction temperature is higher than the ambient temperature. Please calculate the allowed ambient temperature range by using the maximum antenna current and the maximum package thermal resistance. It is the user's responsibility to guarantee that T_J remains always below 110°C.
Supply voltage (V_{DD} and DV_{DD} pads) must be blocked by a 100nF capacitor (to V_{SS}) as close as possible to the chip

Electrical and Switching Characteristics

Parameters specified below are valid only in case the device is used according to Operating Conditions defined on previous page. V_{SS} = DV_{SS} = 0V, V_{DD} = DV_{DD} = 5V, T_j = -40°C to 110°C; unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply current in power down mode	$I_{DDsleep}$			1	5	µA
Supply current excluding antenna current	I_{DDon}			5	10	mA
CAGND level	V_{CAGND}	Note 1	2.35	2.5	2.65	V
Logic signals						
Input logic high	V_{IH}		$0.7V_{DD}$			V
Input logic low	V_{IL}				$0.3V_{DD}$	V
Output logic high	V_{OH}	I_{SOURCE} = 1mA	$0.9V_{DD}$			V
Output logic low	V_{OL}	I_{SINK} = 1mA			$0.1V_{DD}$	V
IN, CLK, EC pull down resistor	R_{PD}	$0.3V_{DD}$	25	50	85	kΩ
PLL						
Antenna capture frequency range	F_{ANT_C}		100		150	kHz
Antenna locking frequency range	F_{ANT_L}		100		150	kHz
Antenna driver						
ANT driver output resistance, full path	R_{AD}	I_{Ant} = 100mA		8	15	Ω
Diagnostic ANT driver threshold “high”	$V_{diagOutH}$		$0.7V_{DD}$			V
Diagnostic ANT driver threshold “low”	$V_{diagOutL}$				$0.3V_{DD}$	V
AM demodulation						
DEMOD_IN common mode range	V_{CM}		V_{SS} + 0.5		V_{DD} - 0.5	V
DEMOD_IN input sensitivity, at gain = 480	V_{sense}	Note 2		0.8	1.4	mV_{pp}
Diagnostic DEMOD_IN threshold	V_{diagIn}		1.0		1.6	V_{pp}

Note 1: AGND is an EM4097 internal reference point. Any external connection except specified capacitor to V_{SS} may lead to device malfunction.

Note 2: Modulating signal 2kHz square wave on 125kHz carrier, within boundaries of V_{CM}.

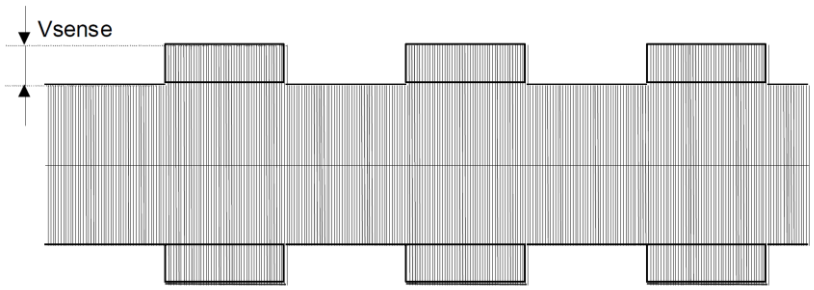

Fig. 5

Timing Characteristics

Parameters specified below are valid only in case the device is used according to Operating Conditions defined on previous page.
V_{SS} = DV_{SS} = 0V, V_{DD} = DV_{DD} = 5V, T = 25°C; unless otherwise specified.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Set-up time after a sleep period (fast start-up)	T_{setF}			25	35	ms
Set-up time after a mode change (slow start-up)	T_{setS}			100	140	ms
AM demodulation: Delay time from input to output	T_{pd}	Modulating signal 2kHz square wave 10mV_{pp}		40	100	µs
Recovery time of reception after antenna modulation	T_{rec}	at f_{Res}= 125kHz Note 1			550	µs
External clock frequency range	f_{ext}		3.2	4.0	4.8	MHz
External clock duty cycle			40		60	%
External clock input capacitance	C_{EC}			5		pF
Maximum clock frequency	f_{max}				1	MHz
Minimum pulse width (CLK) “high”	$t_{W(H)}$		400			ns
Minimum pulse width (CLK) “low”	$t_{W(L)}$		400			ns
Minimum setup time	t_s		50			ns
Minimum hold time	t_h		5			ns

Note 1: The condition is of course that the amplitude on antenna has already reached its steady state by that time (this depends on Q of antenna). See also Application Notes.

Block Diagram

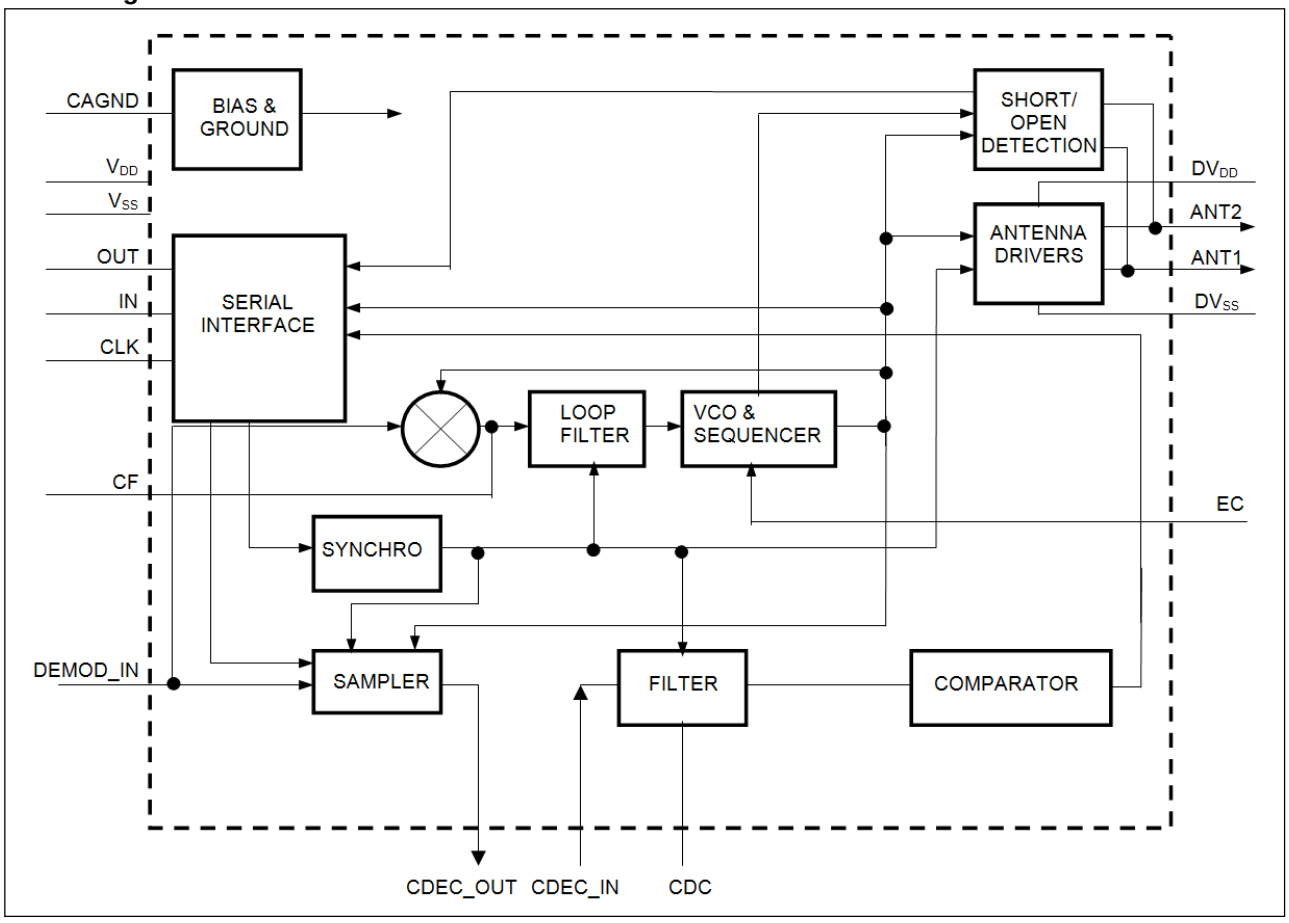

Fig. 6

Functional Description

General

The EM4097 is intended to be used either with an attached antenna circuit and a µcontroller or in an active but non-intelligent antenna configuration. Few external components are needed to achieve DC and RF filtering and power supply decoupling.

A stabilised power supply with sufficient current rating to supply the coil driver has to be provided. Any ripple on V_{SS} causes a modulation of the antenna voltage and therefore a modulation of the received signal at DEMOD_IN. Please note that operating configurations in this document present only elements, which are essential for EM4097 operation. Additional power supply filtering capacitors, which are necessary to filter power supply are not shown.

Serial Interface

Device operation is controlled by 8 bit Configuration Register. This register is written via serial interface. The functionality is as follows:

Serial Interface is controlled by signal CLK. When power supply is applied (Power on Reset) Serial Interface is set in Initial State (beginning of timing on figure 7). The CLK signal has to be low. First pulse on CLK will transition Serial Interface in Command State. In Command State the functionality of the IN and OUT pins changes: IN pin is used to enter 8 bit data, OUT pin is used as diagnostic output. During clock cycles 2 to 9 the Serial Interface receives 8 bit information. The 8 bits are shifted in 8 bit shift register on rising edge of CLK. On the falling edge of pulse 9 the 8 bit information is loaded in Configuration Register. During cycles 10 to 12 the µController gets status information back from the device. The status bits are put on pin OUT after rising edge on signal CLK. With the 13th clock pulse Serial Interface transition in Active State, pins IN and OUT resume their normal function. Additional pulses on pin CLK do not have any influence on EM4097 operation. An Interface Reset is needed to transition Serial Interface back in Initial State.

Interface Reset: A high Signal at the CLK pin and a rising edge at the IN pin causes transition of Serial Interface in Initial State. Interface Reset is accepted in all states of Serial Interface.

Change of EM4097 Configuration register and thus operation of device is done by performing Interface Reset and shifting in new 8 configuration bits.

Power on Reset: After the power is switched on the internal POR circuitry set Serial Interface in Initial State. Power Down bit of Configuration Register is set to 0 (power down mode). EM4097 is thus in inactive sleep mode with low current consumption.

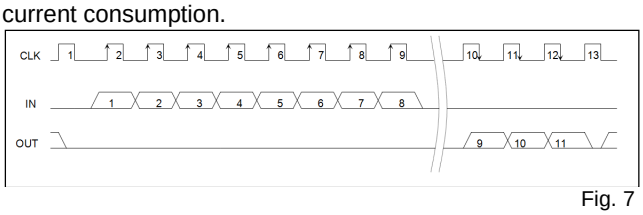

Fig. 7

As explained above the Configuration Register changes its state with the falling edge of clock 9 in the Command Mode. Changing the Power Down bit, changing the gain, the demodulation phase or the clock source causes a delay of about 100ms until the operating points of analog blocks are settled. This time can be reduced to about 25ms if the fast analog start-up has been set. In order to receive a correct diagnostic output an appropriate pause has to be inserted between CLK pulses 9 and 10.
Anyway the chip can be forced to return an answer immediately after sending the 8 configuration bits but the diagnostic data like PLL-Status may be incorrect since the analog operating points are not set yet. See also figure 8, which present possible states of Serial Interface and conditions for transitions between them.

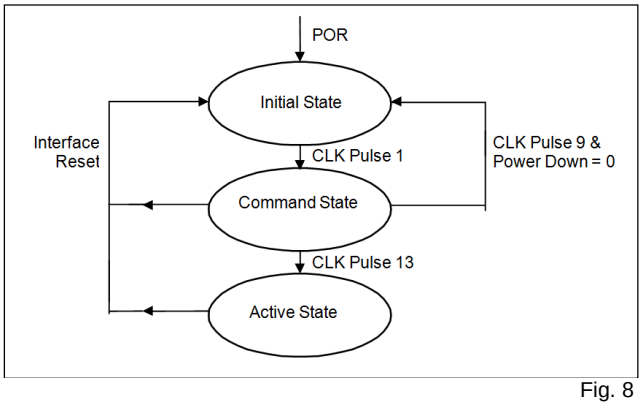

Fig. 8

Configuration Register Definition

Bit #	Description		Reset	if Bit is set to "0"	if Bit is set to "1"
1	Sample Point		0	Amplitude demodulation	Phase demodulation
2	Power Down		0	Power Down	Active
3	EC=1 Bit#4=0	Data Direction	0	Data from Txp at OUT-pin IN pin has no function	Data to Txp with IN-pin OUT pin pulled to VSS
	EC=0 Bit#4=0	Data/Clock		Txp-Data at OUT-pin	Clock at OUT-pin
	EC=X Bit#4=1	Data/Clock		Txp-Data at OUT-pin	Clock at OUT-pin
4	Clock source		0	Internal PLL	External clock
5	Analog start-up		0	no change	fast start-up
6	Gain setting		0	see below	
7	Gain setting		0	see below	
8	Test mode		0	Normal mode	Test mode
9	Antenna Status		0	Correct load	Short circuit
10	Input Status		0	Correct signal	No input signal
11	PLL-Status		0	Locked	Not locked

Bit #1: The relative demodulation phase can be changed with this bit allowing higher tolerances in the transponder to antenna matching.

Bit #2: This bit determines whether the chip is in sleep mode with low power consumption or active. Active mode means the chip is using the current contents Configuration register for operation. Note that there is no answer from the chip after sending the power down bit. This means that on falling edge of bit 9 Serial Interface transition in Initial State if Power Down bit is set to 0.

Bit #3: The meaning of this bit is controlled by the EC pin and bit #4.

If EC is pulled to V_{DD} and bit #4 is 0, the direction of data is switched with this bit, pins IN and OUT are not used at the same time. Depending on the Data Direction bit either the OUT pin is outputting the data sent by the Transponder or the IN pin is modulating the Antenna Driver. When OUT pin is used, IN pin has no influence on antenna drivers (they are always ON independent of IN pin). When IN pin is used OUT pin is always driven to VSS. Such set up allows to connect OUT and IN pin together to achieve a two wire connection in an active antenna configuration (see also figure 13. Typical operating configuration as Active Antenna).

If the EC pin is pulled to V_{SS} or left open and bit #4 is 0, the meaning of Bit #3 is different. Now it switches either the Data Comparator (output of the demodulation chain) or the Clock Reference (signal driving the antenna) divided by 32 to the OUT pin.

In case the "External clock" mode is selected with Bit #4, the EC pin is used for different purpose and the meaning of Bit #3 is independent of this pin. The bit is used for the Data/Clock selection in this case.

The state of this bit does not affect the behaviour of the serial interface; in any case the serial register can be written and read by the IN and OUT pins.

Bit #4: The clock for driving the antenna and demodulating the received signal can be generated by an internal PLL if this bit is set to "0" or by an external source connected to the pin EC if Bit #4 is set to "1". In case the EC-pin is not used it should be left open or connected to VSS.

Bit #5: This decides whether the analog circuitry is doing a fast start-up or not. The settling time can be reduced from about 100ms to about 25ms if parameters like sample point or gain setting have been changed. If fast analog start-up is set it is active from falling edge of pulse 9 to the rising edge of pulse 10 on pin CLK.

Bit #6 & Bit#7: These bits control the gain of the amplifier. By combining both bits the gain can be set in four steps of 6dB. Note that Bit #6 is decreasing the gain by 50% whereas Bit #7 is increasing the gain by 100%. The default state is a gain of 480.

Gain setting

Bit #6	Bit #7	Gain
0	1	960
0	0	480
1	1	240
1	0	120

Bit #8: This bit switches into a test mode when set. The test mode will be left after clock pulse 13 on pin CLK. Therefore the test mode is volatile even if it has been selected by accident. Note that the functionality and pin assignment in this mode is different. It should be avoided in the application.

Bit #9 – Bit#11: These bits are the diagnostic output of the EM4097. The detectable faults are an unlocked PLL (due to antenna mistuning for example), a short circuited connection to the antenna or a signal below a certain threshold. The short circuit detection is done by a voltage level comparison of the antenna driver. If the driver can not pull the output close enough to V_{SS} or V_{DD}, a short circuit is detected and the driver is switched off immediately. This state is steady until the next command is sent. Note that short circuit on antennas driver shall be avoided as the maximum peak current will go beyond absolute maximum ratings. In the case bit #4 is 1 (external clock) the PLL is not used, PLL-status bit is set to 0.

Entering Data in Serial Interface

Figure below presents case where bit with value 1 is entered. IN has to be high at least t_S (50ns) before rising edge of CLK. In the opposite case, not only that data 1 is not accepted also Serial Interface reset might be activated. The position of falling edge is not critical.

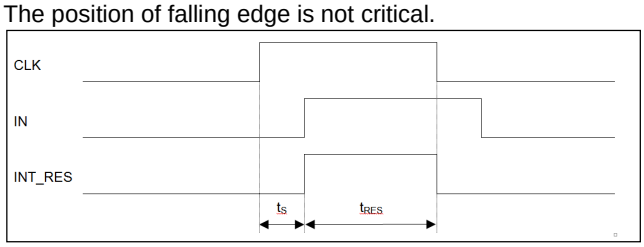

Fig. 9

Interface Reset Timing

As defined in the EM4097 specification, Interface Reset is done when rising edge on IN happens while CLK is high. We recommend that rising edge on IN appears minimum t_S (50ns) after rising edge on CLK. Internal reset signal is active until falling edge on CLK happens. We recommend keeping reset minimum 200ns. Falling edge on pin IN is not important. IN can transition to 0 even before CLK.

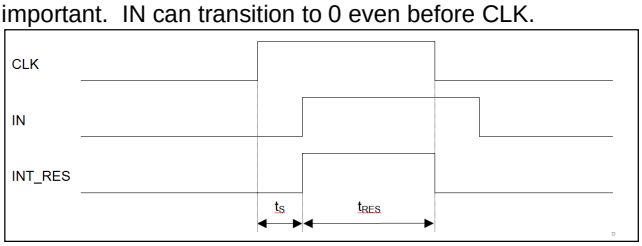

Fig. 10

Interface reset is realised by a FF where low state of CLK is reset and IN is clock signal. Due to this respect of t_S in both cases (before rising edge of CLK to send data and after rising edge of CLK to make Interface reset is important).

Pins IN and OUT in Initial and Active state of Serial Interface

The signal at the IN pin is modulating the antenna signal. A “high” signal switches the antenna driver on, whereas a “low” signal is forcing the antenna driver into tri-state mode to achieve a fast de-energizing of the coil.

Output OUT is behaving according to the setting in Bit #3.

Analog Blocks

The circuit performs the two functions of an RFID basestation, namely: transmission and reception. Transmission involves antenna driving and AM modulation of the RF field. The antenna driver delivers a current into the external antenna to generate the magnetic field.

Reception involves the ASK or PSK demodulation of the antenna signal which is modulated by the transponder. This is achieved by sensing the absorption modulation applied by the transponder.

Transmission

Referring to the block diagram, transmission is achieved by a Phase Locked Loop (PLL) and the antenna driver.

Driver

The antenna driver supplies the reader basestation antenna with the appropriate energy. It delivers current at the resonant frequency which is typically 125 kHz. The current delivered by the driver depends on the Q of the external resonance circuit.

It is strongly recommended that the design of the antenna circuit is done in a way that the maximum peak current of $250mA_p$ is never exceeded (see Typical Operating Configuration for antenna current calculation). Another limiting factor for the antenna current is the limited amount of thermal energy which could be dissipated by the package by radiation and convection. The maximum peak current should be designed in a way that the internal junction temperature does not exceed the maximum junction temperature at allowed maximum ambient temperature. 100% modulation (OOK) is done by switching off the drivers. The antenna driver is protected against antenna DC short circuit to the power supplies. If an short circuit of the antenna or from the driver to ground or supply is detected, the status “Short Circuit” (Bit #9) is set to “1”.

Phase locked loop / External Clock

The clock for the antenna driver is either generated using the integrated PLL or it is connected from outside through the EC pin (External Clock Input) as 4 MHz square wave. The EC clock is divided by 32.

The PLL is composed of the loop filter, the voltage controlled oscillator (VCO) and the phase comparator blocks. By using an external capacitive divider, pin DEMOD_IN gets a divided antenna signal.

The phase of this signal is compared with the signal which is driving the antenna driver. Therefore the PLL is able to lock the carrier frequency to the resonant frequency of the antenna. Depending on the antenna type the resonant frequency of the system can be anywhere in the range from 100kHz to 150kHz. Wherever the resonant frequency is in this range it will be maintained by the phase lock loop.

Reception

The demodulation input signal for the reception block is the voltage sensed at the antenna. The DEMOD_IN pin is used as input to the reception chain. The signal level on the DEMOD_IN input must be lower than V_{DD} - 0.5V and higher than V_{SS} + 0.5V. The input level is adjusted by the use of an external capacitive divider. The additional capacitance of the divider must be compensated by an accordingly smaller resonance capacitor. The AM/PM demodulation scheme is based on the "AM Synchronous Demodulation" technique.

The reception chain is composed of a sample and hold circuit, a DC offset cancellation, a bandpass filter and a comparator. The DC voltage of the signal on DEMOD_IN is set to the AGND voltage by an internal resistor. The AM signal is sampled, synchronised with the VCO. Any DC component is removed from this signal by the CDEC capacitor. Further filtering to remove the remaining carrier signal, as well as high- and low frequency noise, is made by a second order highpass filter and CDC. The amplified and filtered demodulated signal is fed to an asynchronous comparator. By the Sample-Point command the kind of demodulation can be chosen. The phase shift between VCO and sample frequency for both kinds of demodulations is fixed in a way that pure amplitude- and pure phase demodulation is possible. With this technique the EM4097 could demodulate also the phase shift which occurs in certain tuning conditions between the transponder and the antenna circuit.

TXP-Modulation / Reference-CLK

In Active Status either the Transponder modulation information or the Reference-CLK signal is transmitted through the OUT-Pin, but only if the Modulation Bit is not set. The Reference-CLK is the Clock for the ANT1 and ANT2 Clock signal divided by 32, so that the controller can calculate the actual clock signal frequency.

Typical Applications

Read/Write mode (Low Q factor antenna) using internal PLL signal to generate the carrier frequency

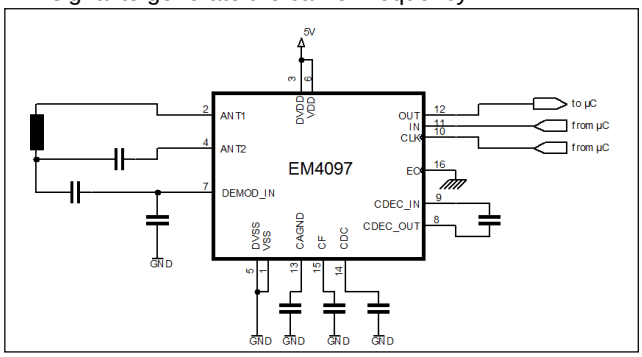

Fig. 11

Read/Write mode (Low Q factor antenna) using external reference signal to generate the carrier frequency

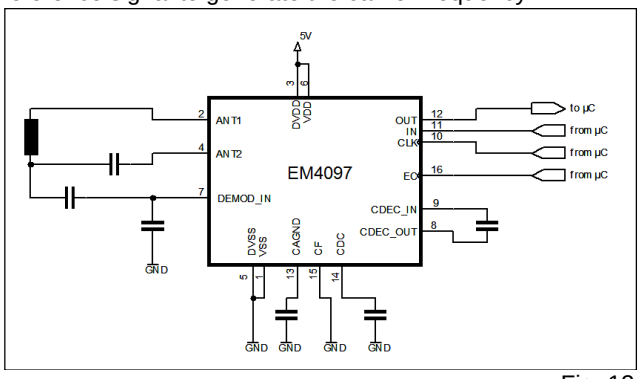

Fig. 12

EM4097 used as active antenna

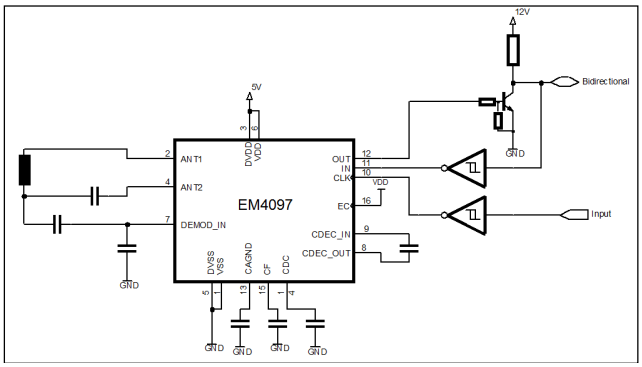

Fig. 13

PCB Layout

Refer to "EM4095 Application Note" (App. Note 404)

Pin Description

SOIC 16 Package

Pin	Symbol	Description	Type
1	V_{SS}	negative supply voltage	power supply
2	ANT1	antenna driver output	output
3	DV_{DD}	positive supply voltage for antenna driver	power supply
4	ANT2	antenna output	output
5	DV_{SS}	negative supply voltage for antenna driver	power supply
6	V_{DD}	positive supply voltage	power supply
7	DEMOD_IN	receiver input	analog input
8	CDEC_OUT	DC blocking capacitor connection “out”	analog signal
9	CDEC_IN	DC blocking capacitor connection “in”	analog signal
10	CLK	µC interface, serial clock input	input (pull down)
11	IN	µC interface, serial data input, modulation pin	input (pull down)
12	OUT	µC interface, serial data output, clock reference	output
13	CAGND	Analog ground	analog signal
14	CDC	DC decoupling capacitor	analog signal
15	CF	PLL loop filter capacitor	analog signal
16	EC	external clock	input (pull down)

Package Information

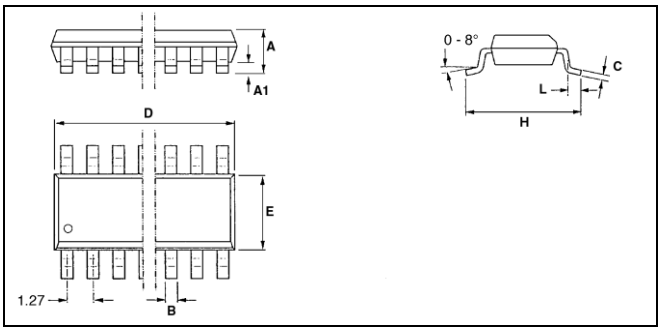

Fig. 13 Dimensions of SO16 Package

	Dimensions in millimeters		
Symbol	**Min.**	**Nom.**	**Max.**
A	1.55	1.63	1.73
A1	0.13	0.15	0.25
B	0.35	0.41	0.49
C	0.19	0.20	0.25
D	9.80	9.93	9.98
E	3.81	3.94	3.99
H	5.84	5.99	6.20
L	0.41	0.64	0.89

Ordering Information

EM4097 V2 SO16 A +

Version

RoHS Compliance
+ = Leadfree
[blank] otherwise

Delivery form
A = Stick
B = Tape & reel

Package
SO16 = SOIC16

Product Support
Check our Web Site under Products/RF Identification section.
Questions can be sent to EMdirect@emmicroelectronic.com